WHAT IS CLAIMED IS:

1. A semiconductor wiring substrate including a semiconductor substrate and a plurality of pieces of wiring formed on the semiconductor substrate, a plurality of chip IPs to be connected to the plurality of pieces of wiring being mounted on said semiconductor wiring substrate, said semiconductor wiring substrate comprising:

an insulating layer formed on the wiring; and

a boundary scan test circuit constituted by a plurality of semiconductor elements provided on said insulating layer, said boundary scan test circuit being respectively connected to the plurality of pieces of wiring.

2. The semiconductor wiring substrate according to claim 1, wherein said boundary scan test circuit is constituted by thin-film transistors.

3. A semiconductor wiring substrate having a semiconductor substrate and a plurality of pieces of wiring formed on the semiconductor substrate, a plurality of chip IPs to be connected to the plurality of pieces of wiring being mounted on said semiconductor wiring substrate, said semiconductor wiring substrate comprising:

an insulating layer formed on the wiring; and

a boundary scan test circuit provided in each of regions where the chip IPs are to be mounted, said boundary scan test circuit being constituted by a plurality of semiconductor elements each having as its active region a portion of the semiconductor substrate of said semiconductor wiring substrate, said boundary scan test circuit having a plurality of connection points respectively connected to the plurality of pieces of wiring.

4. A semiconductor wiring substrate having a semiconductor substrate and a plurality of pieces of wiring formed on the semiconductor substrate, a plurality of chip IPs to be connected to the plurality of pieces of wiring being mounted on said semiconductor wiring substrate, said semiconductor wiring substrate comprising:

an insulating layer formed on the wiring; and

testing pads for testing the chip IPs, said testing pads being formed in a grid pattern on said semiconductor wiring substrate and individually connected to the plurality of pieces of wiring.

5. The semiconductor wiring substrate according to claim 4, wherein said testing pads are formed in a grid pattern over the entire surface of said semiconductor wiring substrate.

6. A semiconductor wiring substrate having a semiconductor substrate and a plurality of pieces of wiring formed on the semiconductor substrate, a plurality of chip IPs to be connected to the plurality of pieces of wiring being mounted on said semiconductor wiring substrate, said semiconductor wiring substrate comprising:

testing pads for testing the chip IPs, said testing pads being formed on said semiconductor wiring substrate and individually connected to the plurality of pieces of wiring,

wherein said testing pads function as power supply pads only at the time of testing.

7. A semiconductor wiring substrate comprising:

a semiconductor substrate on which a plurality of chip IPs are to be mounted; and

a plurality of pieces of wiring formed on said semiconductor substrate to be used only for testing.

8. The semiconductor wiring substrate according to claim 7, further comprising testing pads for testing the chip IPs, said testing pads being formed on said semiconductor wiring substrate,

wherein said pieces of wiring for testing only are connected to said testing pads.

9. The semiconductor wiring substrate according to claim 7, further comprising a multilayer wiring layer formed on said semiconductor substrate by alternately superposing a plurality of wiring layers and a plurality of insulating layers,

wherein said pieces of wiring for testing only are formed in one of the layers in said multilayer wiring layer below the uppermost layer.

10. The semiconductor wiring substrate according to claim 8, wherein said pieces of wiring for testing only are formed in two of said plurality of wiring layers so as to intersect with each other as seen in a plan view, and

wherein conductor portions are formable by dielectric breakdown between said testing pads and said two wiring layers at points of intersection of said pieces of wiring.

11. A semiconductor device comprising:

a semiconductor wiring substrate having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a boundary scan test circuit provided in each of said chip IPs; and

an internal scan chain for an internal scan test, said scan chain being formed in each of said chip IPs and capable of operating simultaneously with said boundary scan test circuit.

12. The semiconductor device according to claim 11, wherein at least one of scanning signal input terminals connected to said internal scan chain is a terminal specially formed separately from said boundary scan test circuit.

13. The semiconductor device according to claim 11, wherein each of in-chip chains in said boundary scan test circuit of said plurality of chip IPs is formed so as to also function as said internal scan chain in the chip IP;

wherein an input-side wiring branch and an output-side wiring branch which respectively branch off from an input-side end portion and an output-side end portion of said boundary scan test circuit are formed in each of said chip IPs;

wherein a scan-in terminal of said internal scan chain is connected to said input-side wiring branch, while a scan-out terminal of said internal scan chain is connected to said output-side wiring branch; and

wherein an input to said in-chip chain can be selected from a signal in said boundary scan test circuit and a signal from said input-side wiring branch.

14. A semiconductor device comprising:

a semiconductor wiring substrate having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a boundary scan test circuit provided in each of said chip IPs;

at least two pieces of wiring formed in the wiring layer of said semiconductor wiring substrate to be used only for testing; and

an input terminal and an output terminal for a boundary scan test connected to said boundary scan test circuit in each of said chip IP and respectively connected to said two pieces or wiring for testing only.

15. The semiconductor device according to claim 14, wherein said boundary scan test circuit in said plurality of chip IPs is formed so as to also function as an internal scan test circuit in said chip IPs:

wherein an input-side wiring branch and an output-side wiring branch which respectively branch off from an input-side end portion and an output-side end portion of said boundary scan test circuit are formed in each of said chip IPs;

wherein a scan-in terminal through which an internal scan test signal is input is connected to said input-side wiring branch;

wherein a scan-out terminal through which a scan test result is output is connected to said output-side wiring branch; and

wherein an input to said in-chip chain can be selected from a signal in said boundary scan test circuit and a signal from said wiring branch.

16. The semiconductor device according to claim 11, wherein said boundary scan test circuit in said plurality of chip IPs is formed integrally with said internal scan chain;

wherein said semiconductor device further comprises first special-purpose wiring which is formed in the wiring layer of said semiconductor wiring substrate, and through which a control signal is supplied to said internal scan chain in each of said chip IPs, and

second special-purpose wiring which is formed in the wiring layer of said semiconductor wiring substrate, and through which signal in said internal scan chain in each of said chip IPs is output;

wherein a scan-in terminal of said internal scan chain in each of said chip IPs is connected to said first special-purpose wiring; and

wherein a scan-out terminal of said internal scan chain in each of said chip IPs is connected to said second special-purpose wiring.

17. A method for testing a semiconductor device including a logic circuit having a boundary scan test function and a built-in self-test (BIST) function, said method comprising:

combining a built-in logic block observer (BILBO) function with the boundary scan test function of the logic circuit; and

making a boundary scan test and a built-in self-test (BIST) on the logic circuit.

18. A method for testing a semiconductor device including a logic circuit having a boundary scan test function and a built-in self-test (BIST) function, said method comprising:

providing a built-in logic block observer (BILBO) function in the logic circuit; and

making a boundary scan test and a BIST on the logic circuit by supplying a linear feedback shift register (LFSR) signal as a boundary scan test signal to the logic circuit and by compressing boundary scan test results.

19. A semiconductor device comprising:

a semiconductor wiring substrate having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a scan test circuit provided in each of said chip IPs, said scan test circuit having a plurality of scan-in terminals and the same number of scan-out terminals as the number of said scan-in terminals; and

a plurality of pieces of wiring formed in the wiring layer of said semiconductor wiring substrate to be used only for testing, a control signal being supplied to said scan test circuit of each of said chip IPs through said pieces of wiring, the number of said pieces of wiring being equal to the number of said scan-in terminals;

wherein said scan-in terminals of said scan test circuit in each of said chip IPs are respectively connected to said pieces of wiring for testing only.

20. The semiconductor device according to claim 19, further comprising a gate connected to each of said scan-in terminals, said gate setting an input to said scan-in terminals to a fixed value when a mode other than a scan test mode is selected.

21. A semiconductor device comprising:

a semiconductor wiring substrate having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a scan test circuit provided in each of said chip IPs, said scan test circuit having a plurality of scan-in terminals and the same number of scan-out terminals as the number of said scan-in terminals; and

a plurality of pieces of wiring formed in the wiring layer of said semiconductor wiring substrate to be used only for testing, a control signal being supplied to said scan test circuit of each of said chip IPs through said pieces of wiring, the number of said pieces of wiring being equal to the number of said scan-out terminals;

wherein said scan-out terminals of said scan test circuit in each of said chip IPs are respectively connected to said pieces of wiring for testing only.

22. The semiconductor device according to claim 21, further comprising a gate connected to each said scan-out terminal and having a high-impedance when a mode other than a scan test mode is selected.

23. A semiconductor device comprising:

a semiconductor wiring substrate having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a scan test circuit provided in each of said chip IPs, said scan test circuit having a plurality of scan-in terminals and the same number of scan-out terminals as the number of said scan-in terminals; and

clock wiring formed in the wiring layer of said semiconductor wiring substrate, said clock wiring being used only for supplying a clock signal to said scan test circuit of each of said chip IPs;

wherein a clock terminal of said scan test circuit in each of said chip IPs is connected to said clock wiring.

24. A semiconductor device comprising:

a semiconductor wiring substrate having a semiconductor substrate and a wiring layer formed on the semiconductor substrate;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto; and

a test controller provided on said semiconductor wiring substrate for the purpose of controlling a circuit in each of said chip IPs.

25. The semiconductor device according to claim 24, wherein said test controller is constituted by a semiconductor element having a portion of said semiconductor substrate as its active region.

26. The semiconductor device according to claim 24, wherein said test controller is provided as a chip IP on said semiconductor wiring substrate.

27. The semiconductor device according to claim 24, wherein, when the circuit in one of said plurality of chip IPs is separately tested by a scan method, if a boundary scan test circuit exists in the circuit in a second one of said chip IPs adjacent to said first one of said chip IPs, said test controller supplies a test pattern from an internal scan chain in the circuit in said first one of said chip IPs and executes an operation for connection to said

boundary scan test circuit to simultaneously make the test on the circuit in said first one of said chip IPs and a test on the wiring between said first one of said chip IPs and said second one of said chip IPs.

28. The semiconductor device according to claim 24, wherein the circuit in each of said chip IPs has a linear feedback shift register (LFSR) function, a multiple input signature register (MISR) function and a BIST function, and

wherein said test controller supplies a signal from a linear feedback shift register (LFSR) to a scan-in terminal of the circuit in each of said chip IPs and makes a multiple input signature register (MISR) take in a signal from a scan-out terminal of the circuit in each of said chip IPs.

29. The semiconductor device according to claim 24, further comprising a function for controlling the power supply voltage to each of said chip IPs, wherein said test controller supplies the power supply voltage only to the circuit in the chip IP subjected to a test among said plurality of chip IPs and stops supply of the power supply voltages to the other chip IPs.

30. A mounting method for a semiconductor device, comprising:

a step (a) of mounting a plurality of chip IPs on a semiconductor wiring substrate having a wiring layer by bonding the chip IPs to the semiconductor wiring substrate;

a step (b) of making a go-no-go test on the plurality of chip IPs; and

a step (c) of substituting another chip IP of the same type for the chip IP determined as a defective one in said step (b), and making the go-no-go test on the substituted chip IP,

wherein said step (c) is repeated until the substituted chip IP is determined as a nondefective one.

FIG. 2

#1 CHIP IP

FIG. 8

#1 CHIP

FIG. 9A

#1 CHIP IP

FIG. 9B

#1 CHIP

FIG. 10

#1 CHIP IP

#2 IPOS DEVICE

FIG. 11

#1 CHIP IP

#2 IPOS DEVICE

FIG. 12

#1 CHIP

#2 IPOS DEVICE

FIG. 13

#1 CHIP

#2 IPOS DEVICE

FIG. 14

#1 CHIP

#2 PERIPHERAL REGION

#3 COMBINATION CIRCUIT

#4 IPOS DEVICE

FIG. 15

#1 CHIP

#2 PERIPHERAL REGION

#3 COMBINATION CIRCUIT

#4 IPOS DEVICE

92 LFSR CIRCUIT

93 COMPRESSOR

FIG. 16

#1 CHIP

#2 CONTROL CIRCUIT

#3 IPOS DEVICE

FIG. 17A

#1 CHIP

#2 CLOCK SIGNAL

#3 IPOS DEVICE

FIG. 17B

#1 CHIP IP

FIG. **18**

#1 CHIP

#2 TEST CONTROLLER

#3 IPOS DEVICE

FIG. **19**

#1 CHIP IP

FIG. **20**

#1 CHIP

#2 IPOS DEVICE

FIG. **21**

#1 CHIP

#2 IPOS DEVICE

125 TEST CONTROLLER

FIG. **22A**

#1 IPOS DEVICE

FIG. **22B**

#1 IPOS DEVICE

FIG. **23A**

#1 TO SUBSEQUENT BSR

#2 INTO CIRCUIT

#3 FROM PRECEDING BSR

FIG. 23B

#1 TO SUBSEQUENT BSR

#2 INSIDE CIRCUIT

#3 FROM PRECEDING BSR

FIG. 24

#1 PATTERN GENERATOR

#2 OBJECT

#3 RESULT COMPRESSOR

#4 CONTROL CIRCUIT

#5 DETERMINATION

#6 END

FIG. 25

#1 SCANNING CIRCUIT

#2 TAP CONTROLLER

FIG. 26

#1 TEST MODE SIGNAL

#2 SCAN-IN

#3 CLOCK SIGNAL

#4 SCAN-OUT